What is claimed is:

[c1] 1.A network processor implemented on a chip, comprising:
means for processing a plurality of protocols including ATM, frame relay, Ethernet, and IP;
said means being programmable using a set of library commands to process additional protocols;
wherein said means comprises an arithmetic logic unit (ALU), a load/store unit (LSU), a preload/bump unit (PBU), a register file unit (RFU), an agent interface, and an internal memory.

[c2] 2.The network processor of claim 1, further comprising a fetch unit and a program sequencer.

[c3] 3.The network processor of claim 1, wherein the ALU performs arithmetic and logic operations on data operands.

[c4] 4.The network processor of claim 1, wherein the LSU performs address calculations in order to address data operands in the internal memory.

[c5] 5.The network processor of claim 4, wherein the LSU calculates an effective address according to one of five available options, including:
(1) effective address is the content of a register from the RFU;
(2) effective address is the sum of content of a first register from the RFU and content of a second register from the RFU;
(3) effective address is the sum of content a first register from the RFU and content of a second register from the RFU after the second register is shifted by a specified number of bits;
(4) effective address is the sum of the content of a register from the RFU and a displacement that occupies a specified number of bits in an instruction word; and
(5) effective address is an absolute address included in the instruction word.

[c6] 6.The network processor of claim 1, wherein the RFU comprises a first register file for a current task and a second register file for preloading register values for a next task.

[c7] 7.The network processor of claim 6, wherein data is read to or written from the first register file based on a comparison between a current task ID and a task ID associated with the first register file.

[c8] 8.The network processor of claim 6, wherein the RFU comprises a third register file for storing register values for the current task that are not stored in the first register file.

[c9] 9.The network processor of claim 8, wherein data is read to or written to the third register file when the current task ID and the task ID associated with the first register file are not the same.

[c10] 10.The network processor of claim 2, wherein the PSU performs decoding of instructions received from the internal memory.

[c11] 11.The network processor of claim 9, wherein the fetch unit controls what instructions are fetched from memory for decoding by the PSU.

[c12] 12.The network processor of claim 8, wherein a task switch is performed by making the next task the current task and preloading a further next task.

[c13] 13.The network processor of claim 12, wherein performance of a task switch includes treating the second register file as the third register file after the task switch.

[c14] 14.The network processor of claim 1, wherein the agent interface allows the network processor to interface to external modules for executing instructions.

[c15] 15.The network processor of claim 14, wherein the external modules include one or more of a CRC module, encryption module, hashing module, and table lookup module.

[c16] 16.The network processor of claim 1, wherein the internal memory for storing program information and data.

[c17] 17.A communications processor implemented on a chip, comprising:
a network processor including means for processing a plurality of protocols including ATM, frame relay, Ethernet, and IP, said means being programmable

using a set of library commands to process additional protocols, wherein said means comprises an arithmetic logic unit (ALU), a load/store unit (LSU), a preload/bump unit (PBU), a register file unit (RFU), an agent interface, and an internal memory;
a protocol processor for controlling the network processor;
wherein the protocol processor performs control plane processing and the network processor performs data plane processing.

[c18] 18.The communications processor of claim 17, wherein the network processor processes instructions by performing a fetch, decode, address, execute, and a write.

[c19] 19.The communications processor of claim 17, wherein the network processor and the protocol processor are ring members on a ring network, and further comprising a plurality of other ring members on the ring network.

[c20] 20.The communications processor of claim 19, wherein the network processor includes a plurality of compounds that share a single ring interface to the ring network.

[c21] 21.The communications processor of claim 20, wherein the compounds include a doorbell agent for controlling the execution sequence of tasks for the network processor.

[c22] 22.The communications processor of claim 20, wherein the compounds include a multireader agent for servicing requests to read data from the internal memory.

[c23] 23.The communications processor of claim 20, wherein the compounds include a message sender agent for sending messages onto the ring network.

[c24] 24.The communications processor of claim 20, wherein the compounds include a DMA agent for sending messages to initiate a DMA controller on the ring network.

[c25] 25.The communications processor of claim 20, wherein the compounds include a CRC agent for performing CRC calculations.

[c26] 26.The communications processor of claim 20, wherein the compounds include a debug module.